

APR 24 2009

JAMES N. HATTEN, Clerk  
By: *[Signature]* Deputy Clerk

IN THE UNITED STATES DISTRICT COURT  
FOR THE NORTHERN DISTRICT OF GEORGIA  
ATLANTA DIVISION

OPTIMUM PROCESSING SOLUTIONS,  
L.L.C., a Georgia Limited Liability  
Company,

Plaintiff,

v.

ADVANCED MICRO DEVICES, INC., a  
Delaware Corporation, BROADCOM  
CORPORATION, a Delaware Corporation,  
FREESCALE SEMICONDUCTOR, INC., a  
Delaware Corporation, INFINEON  
TECHNOLOGIES NORTH AMERICA  
CORPORATION, a Delaware Corporation,  
INTEL CORPORATION, a Delaware  
Corporation, INTERNATIONAL BUSINESS  
MACHINES CORPORATION, a Delaware  
Corporation, STMICROELECTRONICS,  
INC., a Delaware Corporation, SUN  
MICROSYSTEMS, INC., a Delaware  
Corporation, and TEXAS INSTRUMENTS,  
INC., a Delaware Corporation,

Defendants.

1 09 - CV - 1098 **BBM**

COMPLAINT

Plaintiff Optimum Processing Solutions, LLC ("OPS") files this its  
Complaint against Defendants Advanced Micro Devices, Inc., Broadcom

Corporation, Freescale Semiconductor, Inc., Infineon Technologies North America Corporation, Intel Corporation, International Business Machines Corporation, STMicroelectronics, Inc., Sun Microsystems, Inc. and Texas Instruments, Inc. showing this Court as follows.

### **NATURE OF THE ACTION**

#### **1.**

This is an action for patent infringement, arising out of Defendants infringement of a U.S. patent relating to the art of computer processor design. Specifically, this Complaint asserts claims against Defendants arising from their infringement of various claims in U.S. Pat. No. 5,115,497, issued on May 19, 1992, and entitled "OPTICALLY INTRACONNECTED COMPUTER EMPLOYING DYNAMICALLY RECONFIGURABLE HOLOGRAPHIC OPTICAL ELEMENT" (the "'497 Patent"). [A true and correct copy of the '497 Patent is attached hereto as Exhibit A.]

### **THE PARTIES**

#### **2.**

Plaintiff is a limited liability company, organized and existing under the laws of Georgia. Plaintiff's principal place of business is located within this District.

3.

Upon information and belief, Defendant Advanced Micro Devices, Inc. ("AMD") is a corporation organized and existing under the laws of the state of Delaware. Upon information and belief, AMD's principal place of business is located in Sunnyvale, California. AMD's registered agent for service of process in the state of Georgia is CT Corporation, 1201 Peachtree Street, NE, Atlanta, Georgia 30361.

4.

Upon information and belief, Defendant Broadcom Corporation ("Broadcom") is a corporation organized and existing under the laws of the state of Delaware. Upon information and belief, Broadcom's principal place of business is located in Irvine, California. Broadcom's registered agent for service of process in the state of Georgia is National Registered Agents, Inc., 3675 Crestwood Parkway, Suite 350, Duluth, GA 30096

5.

Upon information and belief, Defendant Freescale Semiconductor, Inc. ("FSI") is a corporation organized and existing under the laws of the state of Delaware. Upon information and belief, FSI's principal place of business is located in Austin, Texas. FSI's registered agent for service of process in the state

of Georgia is Corporation Service Company, 40 Technology Parkway South, Suite 300, Norcross, Georgia 30092.

6.

Upon information and belief, Defendant Infineon Technologies North America Corporation ("Infineon") is a corporation organized and existing under the laws of the state of Delaware. Upon information and belief, Infineon's principal place of business is located in San Jose, California. Infineon filed on or about June 23, 2006, a certificate of withdrawal in the state of Georgia and, accordingly, may be served by delivering a copy of the Complaint and Summons upon Corporation Service Company, d/b/a CSC-Lawyers Incorporating Service, 2730 Gateway Oaks Dr., Ste. 100, Sacramento, California 95833.

7.

Upon information and belief, Defendant Intel Corporation ("Intel") is a corporation organized and existing under the laws of the state of Delaware. Upon information and belief, Intel's principal place of business is located in Santa Clara, California. Intel's registered agent for service of process in the state of Georgia is CT Corporation, 1201 Peachtree Street, NE, Atlanta, Georgia 30361.

8.

Upon information and belief, Defendant International Business Machines Corporation ("IBM") is a corporation organized and existing under the laws of the state of Delaware. Upon information and belief, IBM's principal place of business is located in Armonk, NY. IBM's registered agent for service of process in the state of Georgia is CT Corporation, 1201 Peachtree Street, NE, Atlanta, Georgia 30361.

9.

Upon information and belief, Defendant STMicroelectronics, Inc. ("STMicro") is a corporation organized and existing under the laws of the state of Delaware. Upon information and belief, STMicro's principal place of business is located in Santa Clara, California. STMicro's registered agent for service of process in the state of Georgia is CT Corporation, 1201 Peachtree Street, NE, Atlanta, Georgia 30361.

10.

Upon information and belief, Defendant Sun Microsystems, Inc. ("Sun") is a corporation organized and existing under the laws of the state of Delaware. Upon information and belief, Sun's principal place of business is located in Menlo Park, California. Sun's registered agent for service of process in the state

of Georgia is Corporation Service Company, 40 Technology Parkway South, Suite 300, Norcross, Georgia 30092.

11.

Upon information and belief, Defendant Texas Instruments, Inc. ("TI") is a corporation organized and existing under the laws of the state of Delaware. Upon information and belief, TI's principal place of business is located in Dallas, Texas. TI's registered agent for service of process in the state of Georgia is Corporation Process Company, 328 Alexander Street, Suite 10, Marietta, GA 30060.

**JURISDICTION AND VENUE**

12.

This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and/or 1338.

13.

This Court has personal jurisdiction over the Defendants pursuant to O.C.G.A. § 9-10-91.

14.

Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and/or 1400.

**OPERATIVE FACTS**

**THE PATENT-IN-SUIT**

15.

OPS is the owner by assignment of all right, title, and interest in the '497 Patent.

16.

The '497 Patent describes a novel method that optimizes the simultaneous operation of execution elements in a computer processor in a multiple instruction environment. Among other things, the '497 Patent discloses a basic computer comprised of a memory for holding a sequence of instructions to be executed; logic for accessing the instructions in sequence; logic for determining for each instruction the function to be performed and the effective address thereof; a plurality of individual execution elements on a common support substrate optimized to perform certain logical sequences employed in executing the instructions; and element selection logic that: (i) determines the function to be performed for each instruction, (ii) determines the class of each function, and (iii) causes the instruction to be executed by those elements that perform the associated the logical sequences in an optimum manner.

17.

In a preferred embodiment of the '497 Patent, the element selection logic accepts dynamic inputs designating changes in the operating environment of the computer and changes the elements that execute each instruction to optimize execution based upon the present dynamic conditions.

18.

In another preferred embodiment, the '497 Patent also provides that the execution elements can comprise individual arithmetic and logic units contained on a single central processor unit chip or the elements can comprise individual reduced instruction set computers contained on a single central processor unit chip.

19.

Claim 1 of the '497 Patent provides:

1. In a computer including a memory for holding a sequence of instructions to be executed logic for accessing the instructions in sequence, logic for determining for each instruction a function to be performed and an effective address thereof, and logic for executing each instruction, the improvement wherein:

(a) the logic for executing instructions comprises:

a plurality of individual elements on a common support substrate optimized to perform certain logical sequences employed in executing instructions; and

b) the computer comprises:

element selection logic means connected to the logic determining the function to be performed for each instruction, for determining a class of each function and for causing the instruction to be executed by those of said elements which perform those of said logical sequences affecting the instruction execution in an optimum manner

'497 Patent, Col. 8, ll. 5-23

20.

Similarly, Claim 11 of the '497 Patent provides:

11. In a computer including a memory for holding a sequence of instructions to be executed, logic for accessing the instructions in sequence, logic for determining for each instruction a function to be performed and an effective address thereof, and logic for executing each instruction, a method of operation by said computer, wherein said logic for executing each instruction comprises a plurality of individual elements on a common support substrate with each

element optimized to perform certain logical sequences employed in executing instructions, said method comprising for each instruction the steps of:

- (a) determining the function to be performed;
- (b) determining a class of each function;
- (c) causing the instruction to be executed by those elements which perform the associated logical sequences affecting the instruction execution in an optimum manner.

'497 Patent, Col. 9, l. 5- Col. 10, l. 4.

21.

And Claim 16 provides:

16. A computer comprising:

- (a) a memory for holding a sequence of instructions to be executed;
- (b) logic for accessing said instructions in sequence;
- (e) logic for determining for each said instruction a function to be performed and an effective address thereof;
- (d) a plurality of individual elements on a common support substrate optimized to perform certain logical sequences employed in executing said instructions;

and,

- (e) element selection logic means connected to said logic determining the function to be performed for each said instruction for determining a class of each function and for causing the instruction to be executed by those of said elements which perform those of said logical sequences affecting the instruction execution in an optimum manner.

'497 Patent, Col. 11, ll. 7-34.

#### THE INFRINGING PRODUCTS

#### Defendant AMD's Products

#### 22.

Defendant AMD, within the United States, manufactures, uses, offers for sale, or sells computer processor chips, including the Turion and Phenom, (collectively, the "AMD Chips"). The AMD Chips, among other things, have an architecture that contains, on a single substrate, multiple execution elements. These elements include an integer execution unit and floating point execution unit, which logic within the AMD Chips utilize to optimize the execution of instructions. In addition, the AMD Chips' architecture further optimizes the execution of instructions by dynamic scheduling and speculative execution.

23.

The AMD Chips contain each limitation set forth in at least claims 11 and 16 of the '497 Patent.

24.

Defendant AMD does not have a license or other authorization to practice the claims set forth in the '497 Patent.

Defendant Broadcom's Products

25.

Defendant Broadcom, within the United States, manufactures, uses, offers for sale, or sells computer processor chips, including the BCM1480 and BCM1455, (collectively, the "Broadcom Chips"). The Broadcom Chips, among other things, have an architecture that contains multiple execution elements on a single substrate. These elements include an execution unit and a floating point unit, which logic within the Broadcom Chips utilizes to optimize the execution of instructions.

26.

The Broadcom Chips contain each limitation set forth in at least claims 11 and 16 of the '497 Patent.

27.

Defendant Broadcom does not have a license or other authorization to practice the claims set forth in the '497 Patent.

Defendant Freescale's Products

28.

Defendant Freescale, within the United States, manufactures, uses, offers for sale, or sells computer processor chips, including the "i.mx51" and "PowerQuicIII," (collectively, the "Freescale Chips"). The Freescale Chips, among other things, have an architecture that contains multiple execution elements on a single substrate, which are optimized to perform certain types of instructions.

29.

The Freescale Chips contain each limitation set forth in at least claims 11 and 16 of the '497 Patent.

30.

Defendant Freescale does not have a license or other authorization to practice the claims set forth in the '497 Patent

Defendant Infineon's Products

31.

Defendant Infineon, within the United States, manufactures, uses, offers for sale, or sells computer processor chips, including the "XC2000," "XE166," and "XC166," (collectively, the "Infineon Chips"). The Infineon Chips, among other things, have an architecture that contains multiple execution elements on a single substrate, including an ALU unit and MAC unit, which logic within the Infineon Chips utilizes to optimize the execution of instructions.

32.

Each of the Infineon Chips contains each limitation set forth in at least claims 11 and 16 of the '497 Patent.

33.

Defendant Infineon does not have a license or other authorization to practice the claims set forth in the '497 Patent

Defendant Intel's Products

34.

Defendant Intel, within the United States, manufactures, uses, offers for sale, or sells computer processor chips, including the "Quad-Core" and "Core2Duo," (collectively, the "Intel Chips"). The Intel chips, among other things, have an architecture that contains multiple execution elements on a single

substrate, which are optimized to perform certain types of instructions. In particular, the Intel Chips utilize wide dynamic execution to optimize the execution of instruction by those execution elements.

35.

The Intel Chips contain each limitation set forth in at least claims 11 and 16 of the '497 Patent.

36.

Defendant Intel does not have a license or other authorization to practice the claims set forth in the '497 Patent.

Defendant IBM's Product

37.

Defendant IBM, within the United States, manufactures, uses, offers for sale, or sells computer processor chips, including the Cell (the "IBM Cell Chip"), which utilizes IBM's Cell Broadband Engine Architecture, and a modified version of its PowerPC multiprocessor chip (the "IBM Xbox Chip") designed for use in the Microsoft Xbox 360 (collectively, the IBM Cell Chips and the IBM Xbox Chips are referred to as the "IBM Chips"). The IBM Chips, among other things, have an architecture that contains multiple execution elements on a single substrate. In particular, each IBM Cell Chip contains a power processor element

("PPE") and eight synergistic processor elements ("SPEs"), which logic within the IBM Cell Chip utilizes to optimize the execution of instructions. Similarly, each IBM Xbox Chip contains 3 CPU cores, each of which is comprised of a fixed point pipe that handles add/sub, cmp, logical ops, and rotate and multiply/divide and a VMX/FPU unit that executes floating point instructions, which logic within the IBM Xbox Chip utilizes to optimize the execution of instructions.

38.

The IBM Cell Chips contain each limitation set forth in at least claims 1 and 11 of the '497 Patent.

39.

The IBM XBox Chips contain each limitation set forth in at least claims 11 and 16 of the '497 Patent.

40.

Defendant IBM does not have a license or other authorization to practice the claims set forth in the '497 Patent.

Defendant STMicro's Product

41.

Defendant STMicro, within the United States, manufactures, uses, offers for sale, or sells computer processor chips, including the "ST140," (collectively,

2472521 v05

the “STMicro Chips”) The STMicro Chips, among other things, have an architecture that contains multiple execution elements on a single substrate, which logic within the STMicro Chips utilizes to optimize the execution of instructions.

42.

The STMicro Chips contain each limitation set forth in at least claims 11 and 16 of the ‘497 Patent.

43.

Defendant STMicro does not have a license or other authorization to practice the claims set forth in the ‘497 Patent.

Defendant Sun’s Product

44.

Defendant Sun, within the United States, manufactures, uses, offers for sale, or sells computer processor chips, including the “UltraSPARCHIV+,” (collectively, the “Sun Chips”). The Sun Chips, among other things, have an architecture that contains multiple execution elements on a single substrate, which logic within the Sun Chips utilizes to optimize the execution of instructions.

45.

The Sun Chips contain each limitation set forth in at least claims 11 and 16 of the '497 Patent.

46.

Defendant Sun does not have a license or other authorization to practice the claims set forth in the '497 Patent.

Defendant TI's Products

47.

Defendant TI, within the United States, manufactures, uses, offers for sale, or sells computer processor chips, including the "ARM Cortex A8" and "ARM Cortex A9," (collectively, the "TI Chips"). The TI chips, among other things, have an architecture that contains multiple execution elements on a single substrate, which logic within the TI Chips utilizes to optimize the execution of instructions.

48.

Each of the TI Chips contains each limitation set forth in at least claims 11 and 16 of the '497 Patent.

49.

Defendant TI does not have a license or other authorization to practice the claims set forth in the '497 Patent.

DEFENDANT INTEL'S KNOWLEDGE OF THE '497 PATENT

50.

Defendant Intel and OPS's predecessor-in-interest, the California Institute of Technology ("Caltech") entered into an agreement effective May 1, 2001, (the "Subscription Agreement").

51.

Under the provisions of the Subscription Agreement, Caltech agreed to provide Defendant Intel with the "ability and easily to take a non-exclusive license to certain of Caltech's patents and inventions."

52.

To effectuate this purpose, the Subscription Agreement granted Intel the option to review certain intellectual property assigned to Caltech and obtain a license to such intellectual property upon the payment of a predetermined fee.

53.

On or about August 16, 2001, Caltech provided Defendant Intel with a list of patents (the "Option Patents") for its review pursuant to the Subscription Agreement and access to a password protected website for the review of materials related to the Option Patents. Caltech included the '497 Patent in the Option Patents provided to Defendant Intel for its review pursuant to the Subscription Agreement.

54.

On or about March 24, 2006, Defendant Intel requested an extension of time to review the Option Patents that Caltech provided pursuant to the Subscription Agreement, stating that Defendant Intel was “slowly, but surely, making its way through” the patents. Caltech agreed to extend the option date under the Subscription Agreement until June 1, 2006.

55.

Defendant Intel did not exercise its right granted by the Subscription Agreement to obtain a non-exclusive license of the ‘497 Patent.

56.

Defendant Intel had knowledge of the claims contained within the ‘497 Patent prior to Defendant Intel’s design of the Intel Chips. Upon information and belief, Defendant Intel knew or should have known that the Intel Chips infringed at least one claim of the ‘497 Patent at that time.

57.

All conditions precedent to the assertion of the claims set forth in this Complaint have been satisfied or waived.

COUNT ONE

AMD'S INFRINGEMENT OF THE '497 PATENT

58.

OPS incorporates by reference as if fully set forth herein the averments contained within Paragraphs 1-3, 12-24, and 57.

59.

By reason of some or all of the foregoing, Defendant AMD has infringed at least one claim of the '497 Patent.

60.

OPS has suffered damages as the direct and proximate result of Defendant AMD's infringement of the '497 Patent.

COUNT TWO

BROADCOM'S INFRINGEMENT OF THE '497 PATENT

61.

OPS incorporates by reference as if fully set forth herein the averments contained within Paragraphs 1-2, 4, 12-21, 25-27, and 57.

62.

By reason of some or all of the foregoing, Defendant Broadcom has infringed at least one claim of the '497 Patent.

63.

OPS has suffered damages as the direct and proximate result of Defendant Broadcom's infringement of the '497 Patent.

COUNT THREE

FREESCALE'S INFRINGEMENT OF THE '497 PATENT

64.

OPS incorporates by reference as if fully set forth herein the averments contained within Paragraphs 1-2, 5, 12-21, 28-30, and 57.

65.

By reason of some or all of the foregoing, Defendant Freescale has infringed at least one claim of the '497 Patent.

66.

OPS has suffered damages as the direct and proximate result of Defendant Freescale's infringement of the '497 Patent.

COUNT FOUR

INFINEON'S INFRINGEMENT OF THE '497 PATENT

67.

OPS incorporates by reference as if fully set forth herein the averments contained within Paragraphs 1-2, 6, 12-21, 31-33, and 57.

68.

By reason of some or all of the foregoing, Defendant Infineon has infringed at least one claim of the '497 Patent.

69.

OPS has suffered damages as the direct and proximate result of Defendant Infineon's infringement of the '497 Patent.

COUNT FIVE

INTEL'S INFRINGEMENT OF THE '497 PATENT

70.

OPS incorporates by reference as if fully set forth herein the averments contained within Paragraphs 1-2, 6, 12-21, 34-36, and 49-57.

71.

By reason of some or all of the foregoing, Defendant Intel has infringed at least one claim of the '497 Patent.

72.

By reason of some or all of the foregoing, Defendant Intel's infringement of at least one claim of the '497 Patent was willful.

73.

OPS has suffered damages as the direct and proximate result of Defendant Intel's infringement of the '497 Patent.

COUNT SIX

IBM'S INFRINGEMENT OF THE '497 PATENT

74.

OPS incorporates by reference as if fully set forth herein the averments contained within Paragraphs 1-2, 6, 12-21, 37-40, and 57.

75.

By reason of some or all of the foregoing, Defendant IBM has infringed at least one claim of the '497 Patent.

76.

OPS has suffered damages as the direct and proximate result of Defendant IBM's infringement of the '497 Patent.

COUNT SEVEN

STMICRO'S INFRINGEMENT OF THE '497 PATENT

77.

OPS incorporates by reference as if fully set forth herein the averments contained within Paragraphs 1-2, 6, 12-21, 41-43, and 57.

78.

By reason of some or all of the foregoing, Defendant STMicro has infringed at least one claim of the '497 Patent.

79.

OPS has suffered damages as the direct and proximate result of Defendant STMicro's infringement of the '497 Patent.

COUNT EIGHT

SUN'S INFRINGEMENT OF THE '497 PATENT

80.

OPS incorporates by reference as if fully set forth herein the averments contained within Paragraphs 1-2, 6, 12-21, 44-46, and 57.

81.

By reason of some or all of the foregoing, Defendant Sun has infringed at least one claim of the '497 Patent.

82.

OPS has suffered damages as the direct and proximate result of Defendant Sun's infringement of the '497 Patent.

COUNT NINE

TI's Infringement of the '497 Patent

83.

OPS incorporates by reference as if fully set forth herein the averments contained within Paragraphs 1-2, 6, 12-21, 47-49, and 57.

84.

By reason of some or all of the foregoing, Defendant TI has infringed at least one claim of the '497 Patent.

85.

OPS has suffered damages as the direct and proximate result of Defendant TI's infringement of the '497 Patent.

WHEREFORE, OPS prays that this Court:

- (1) Enter judgment in favor of OPS and against Defendants for infringement of the '497 Patent;
- (2) Award damages to OPS in an amount to be proven at trial for infringement of the '497 Patent, pursuant to 35 U.S.C. § 284;
- (3) Award enhanced damages against Defendant Intel and to OPS in amount equal to three times OPS's damages for infringement of the '497 Patent based upon Defendant Intel's willful infringement and/or bad faith, pursuant to 35 U.S.C. § 284;
- (4) This case be tried before a jury; and
- (5) OPS have such other and further relief as the Court deems just and proper, premises considered.

This 24th day of April, 2009.

Respectfully submitted,

MORRIS, MANNING & MARTIN, LLP

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